High Performance RF Passive Integration on Si Smart Substrate

DONG-WOOK KIM, IN-HO JEONG, HO-SUNG SUNG, TONG-OOK KONG, JONG-SOO LEE, CHOONG-MO NAM AND YOUNG-SE KWON*

Telephus Inc.

25-11 Jang-dong, Yuseong-gu, Taejeon, 305-343, Korea

* Dept. of EE, KAIST

373-1 Kusong-dong, Yuseong-gu, 305-701, Taejeon, Korea

Abstract — **To achieve cost and size reduction, we developed low cost manufacturing technology for RF substrate and high performance passive process technology for RF IPDs (Integrated Passive Devices). The fabricated substrate is conventional 6" Si wafer with SiO_2 thickness of 25μm on the surface. This substrate showed the very good insertion loss of 0.03dB/mm at 4GHz, including conductive metal loss, in case of 50Ω coplanar transmission line (W=50μm, G=20μm). Using BCB (Benzo Cyclo Butene) interlayer and 10μm Cu plating process, we made a high Q circular spiral inductor on Si that had the record maximum quality factor of more than 120. The fabricated inductor library showed the maximum quality factor range of 30~120 or more, depending on geometrical parameters and inductance values of 0.35~31.5nH. The small-size RF IPDs were fabricated on thick oxide Si substrate for the applications such as FEMs (Front End Modules) and high-speed wireless LANs and they showed very good performances. These substrate and passive process technologies will be widely utilized in hand-held RF module and system requiring low cost solution and strict volumetric efficiency.**

I. INTRODUCTION

Silicon substrate is known to have a lot of benefits of cheap material, good thermal conductivity, stable and mature process technology, but its utilization has been limited to low frequency region in the fast growing and flourishing wireless market by large signal loss due to conducting substrate and RF signal leakage due to parasitic substrate capacitance. There have been many attempts to use cheap Si wafer as RF substrate. They could be a method to control the doping density to make Si substrate have high resistivity in high frequency region [1], a method to form 9μm SiO_2 layer on Si substrate [2], a method to coat 10μm polyimide layer on Si substrate [3], and so on. All these approaches did not provide remarkable benefits in terms of cost effectiveness and microwave performance.

Usually insulating property of SiO_2 layer on high conductive Si substrate is used for isolation, and effective operation of this SiO_2 layer in RF applications requires it to be thick, in order to isolate the underlying Si substrate capacitively. In the economic and manufacturing considerations, new method to reduce the fabrication cost and the time required to grow thick oxide is required, and so porous silicon technique can be considered as a potential solution. In porous material, the lattice has a large number of its atoms removed electrochemically, producing honeycomb-like structure. Initial work applying porous technique to RF applications took advantage of the oxidation process of the porous silicon layer [4]. More recently, the highly insulating property of porous silicon was used to alleviate the stresses generated as a result of the difference in thermal expansion coefficients of the oxidized porous layer and Si substrate [5]. All these researches were done in university laboratories and their RF performances were not fully optimized partially because the front side process could not support the high quality RF substrate.

In this paper we will provide mass-producible 6" Si substrate with 25μm oxide thickness for RF applications. This RF substrate is called smart substrate at our side, though technical terminologies such as SOPS (Selectively Oxidized Porous Silicon) or OPS have been already used in former work [4]. Also high performance passive process using Cu metal layers and BCB interlayer will be provided to make the most of high quality substrate. This process is low cost and high performance manufacturing process, compared to conventional process. With both the substrate technology and the passive process technology, high Q inductors and several IPDs including diplexer were fabricated. Their measured RF performances will be provided.

II. Si SMART SUBSTRATE AND RF PASSIVE MANUFACTURING PROOCESS

Si is the most stable and reliable semiconductor material in the world and has been utilized in a lot of electronic applications. Unlike semi-insulating GaAs or InP, silicon has typically been forced to rely upon the insulating properties of SiO_2 for isolation. Thin SiO_2 layer cannot isolate capacitively devices on Si substrate. Also

0-7803-7239-5/02/$10.00 © 2002 IEEE

the signal loss at high frequency range is not so good compared to GaAs because of its highly conducting property. These make it difficult to use Si technology for RF applications. To overcome these limitations of Si wafer, we formed very thick oxide layer on top of Si. The reproducible and reliable oxide thickness is 25μm, and the available maximum thickness is 35μm. The time to make thick oxide layer is very short, and so the manufacturing cost is low. This smart substrate is RF substrate that can enjoy full benefits of Si material.

Uniform oxide layer of 25μm or greater can be made on the whole surface of 6" silicon wafer. The thick oxide layer can be also made selectively through thin dielectric masking process. The smart substrate with selective thick oxide pattern is shown in Figure 1. This substrate is very flat (surface roughness <18Å) enough to make fine feature of 1μm. The record oxide thickness and processing time lead to a revolutionary low loss and low cost solution for RF thin film substrate.

To take full advantages of low loss characteristic of Si smart substrate, we developed passive integration process using Cu metallization and BCB interlayer. Cu metal is optimal choice for low conductive metal loss and high-speed operation. We used 10μm Cu plating process for low loss inductor fabrication and interconnection. NiCr was used for resistor and SiNx dielectric material was employed as interlayer insulator of MIM(Metal-Insulator-Metal) capacitor. Total two Cu metal layers and one dummy Cu layer were used for NiCr contact, bottom and top metal formation of MIM capacitor, spiral inductor patterning and element interconnection.

Photosensitive BCB material was used as interlayer between first Cu metal and plated Cu metal in this work. Photo-BCB had been originally developed for use in microelectronics such as MCM (Multi Chip Module) and flat panel display. Because the photo-BCB has a lot of attractive properties such as processing compatibility with existing IC manufacturing techniques, low moisture uptake, low cure temperature, low dielectric constant, low RF loss and etc., it was adopted in our process. The BCB layer of 4.5μm was used for interlayer applications and the layer of 4.5μm was used for final passivation.

The insertion loss of 50Ω coplanar transmission line (W=50μm, G=20μm) fabricated on high quality Si smart substrate of 25μm oxide thickness using Cu-BCB passive process was 0.03dB/mm at 4GHz, including conductive metal loss. The transmission line also showed high performance up to more than 10GHz. The insertion loss was below 0.1dB/mm up to 15GHz. It was much superior to that of expensive HRS(High Resistivity Silicon, 7Kohm-cm) substrate. Table 1 shows the comparison data of transmission line losses obtained from this work and other research results.

III. HIGH Q INDUCTOR AND PASSIVE LIBRARY

The on-chip inductors, which were one of the major technological challenges, were fabricated using 10μm Cu thickness on 6" Si smart substrate of 25μm SiO_2 thickness. The fabricated inductors had 10μm line and 10μm spacing. They showed the maximum quality factor range of 30~120 or greater, depending on geometrical parameters and inductance values of 0.35~31.5nH. The inductors also showed high quality factors in broadband frequency range. For example, 1.05nH Cu circular spiral inductor with 1.5 turns had the quality factor of more than 50 up to 16GHz and the maximum two-port quality factor of more than 120 at 7.75GHz, which is the highest value that has been achieved on Si wafer. Figure 2 is the photograph of a CPW circular spiral inductor with multi-turns on Si smart substrate.

We have measured 96 rectangular spiral inductors (microstrip-like) and 72 circular spiral inductors (CPW structures) and established inductor library for them. Figure 3 shows the equivalent circuit model of spiral inductor made on Si smart substrate. The model includes shunt series RC networks at both of inner side and outer side of the inductor. The shunt R expresses conducting nature of Si substrate underneath the thick SiO_2 layer. The two-port quality factor is very difficult to measure directly and so it is extracted from the equivalent circuit model data that is fitted to the measured data accurately. Figure 4 shows the maximum quality factor distribution of CPW circular spiral inductors with the inductance value and geometry variation. As shown in Figure 4, in case of inductance values less than 10nH that are commonly used in RFICs, the maximum quality factors are more than 45. Different geometry factors lead to different frequency characteristics and quality factor performances, although they have very similar inductance values.

These substrate technology and high Q inductor technology have the potential to push Si applications well into the 10GHz range and also to broaden the area of IPDs up to 10GHz or above.

IV. Si INTEGRATED PASSIVE DEVICES FOR RF APPLICATIONS

MIM capacitors and thin film NiCr resistors for RF applications can be also integrated on Si smart substrate, because of its extremely flat surface. Using high quality passive devices, we fabricated small-size low pass filter, diplexer and wideband balun for FEM and high-speed wireless LAN applications. These devices can be wafer-level-packaged using PbSn solder ball bumping of 170μm or 300μm diameter for ultra small form factor.

Figure 5 shows the measured data of 1800MHz low

pass filter for Tx path of FEM application. The low insertion loss of 0.36dB and the high harmonic attenuation of more than 30dB were obtained. The measured performance of another key component, diplexer is shown in Figure 6. The insertion losses of 0.5dB in GSM band and 0.6dB in DCS band were obtained and the band rejection level was more than 25dB. These two IPDs could be applied to dual-band and tri-band FEM applications.

Figure 7 shows the photograph of the fabricated wideband balun for 5GHz wireless LAN applications. The measured data are shown in Figure 8. The insertion loss was measured to be 0.5~0.8dB, and the obtained amplitude and phase imbalances were less than 0.3dB and 2° in the 5.2~5.8GHz, respectively.

All these Cu-based IPDs have much superior current handling capability to Au-based devices or Al-based devices commonly used in wireless semiconductor industry and also show high RF performances, and therefore the wafer-based RF IPDs will be the optimal choice for FEM applications of handsets and high-speed wireless applications that require really low cost and small size components.

V. Conclusion

There have been many researches on RF passive integration on Si wafer for low cost and mass-producible process. However, they have not provided satisfactory solutions and the results have not been utilized in commercial industry. To meet the requirement of cost and size reduction, we developed low cost manufacturing technology for RF substrate and high performance passive process technology for RF IPDs by forming thick oxide on Si wafer and using Cu metal and BCB interlayer material. The fabricated substrate of 25μm oxide thickness showed good CPW transmission line loss of 0.03dB/mm at 4GHz, including conductive metal loss. The transmission line loss was less than 0.1dB/mm up to 15GHz. With the well-developed substrate process and passive integration process, we obtained high Q inductors on Si wafer, which showed the maximum quality factor range of 30~120 or more, depending on inductance values of 0.35~31.5nH. Especially the inductors showed high quality factors in broadband frequency range. We fabricated small-size RF IPDs for FEM applications and 5GHz wireless applications. They also showed good RF performances and volumetric efficiencies simultaneously. These thick oxide technology and high performance passive integration technology will push the RF operating window of Si wafer well into 10GHz and broaden the area of IPDs, which has been limited to several hundred MHz, up to more than 10GHz. Finally the developed technologies from our work will be widely utilized in hand-held modules and systems requiring stringent size reduction and tough cost reduction.

References

[1] A.C. Reyes, " Silicon as Microwave Substrate," *in IEDM Tech. Digest*, pp. 1759-1762, 1995

[2] H. Sakai, " A New Millimeter-Wave IP-Chip on Silicon Substrate," *in Asia Pacific Microwave Conference*, pp. 291-294, 1994

[3] B.K. Kim, B.K. Ko, and K. Lee, " Monolithic Planar Inductor and Waveguide Substrate on Silicon with Performance Comparable to Those in GaAs MMIC," *in IEDM Tech. Digest*, pp. 717-720, 1995

[4] Choong-Mo Nam and Young-Se Kwon, " High Performance Planar Inductor on Oxidized Porous Silicon(OPS) Substrate," IEEE Microwave Guided Wave Letters, vol. 7, no. 8, pp. 236-238, 1997

[5] Han-Su Kim, Dawei Zheng, A. J. Becker and Ya-Hong Xie, " Spiral Inductors on Si p/p$^+$ Substrate with Resonant Frequency of 20GHz," IEEE Electron Device Letters, vol. 22, no. 6, pp. 275-277, 2001

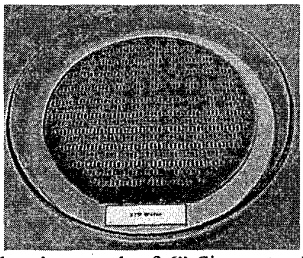

Figure 1. The photograph of 6" Si smart substrate with selective thick oxide definition

Insertion loss (dB/mm)	Dielectric material & thickness	Signal line metal	Substrate	Ref.
0.17 @ 4GHz	SiO_2 (0.9μm)	Al (1μm)	HRS (4KΩ-cm)	IEEE EDL 1991
0.19 @ 4GHz	Polyimide (10μm)	Al (4μm)	Silicon (20Ω-cm)	IEDM 1995
0.2 @ 4GHz	-	Al (1.25μm)	HRS (10KΩ-cm)	IEEE MGWL 1999
0.1 @10GHz	SiO2 (0.1μm) Polysilicon (0.6μm)	Al (1μm)	HRS (10KΩ-cm)	IEEE MGWL 1999
0.05 @ 4GHz	-	Au (5μm)	Pyrex	Exp. data
0.03 @ 4GHz	**thick oxide (25μm)**	**Cu (10μm)**	**Silicon (8Ω-cm)**	**This work**

Table 1. The insertion loss comparison of transmission lines obtained from this work and other research results.

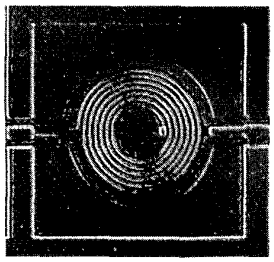

Figure 2. The photograph of CPW circular spiral inductor (inner diameter=175μm, turns=6.5, W=10μm, S=10μm)

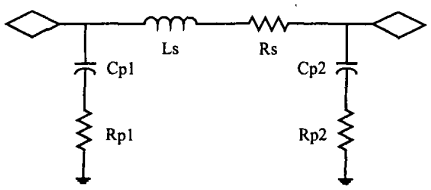

Figure 3. The equivalent circuit model of spiral inductor on Si smart substrate

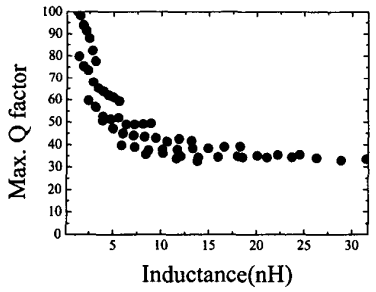

Figure 4. Maximum quality factor distribution with inductance values of CPW circular spiral inductors

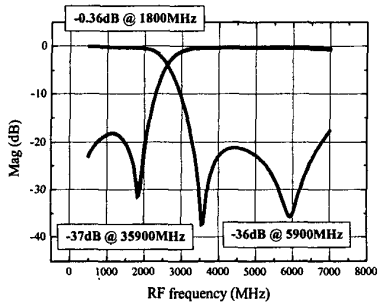

Figure 5. The measured characteristics of 1800MHz low pass filter on Si smart substrate

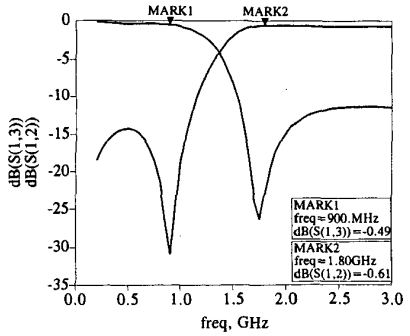

Figure 6. The measured data of GSM/DCS diplexer

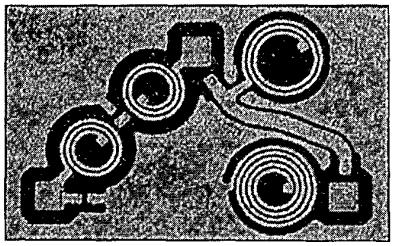

Figure 7. The photograph of 5GHz wideband balun

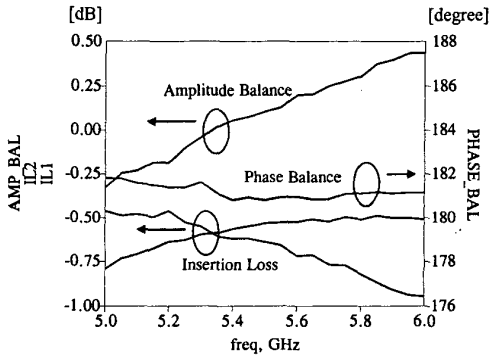

Figure 8. The measured performance of wideband balun